Faculty of Science and Technology
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Field Testing Architecture for Delay Degradation Prediction

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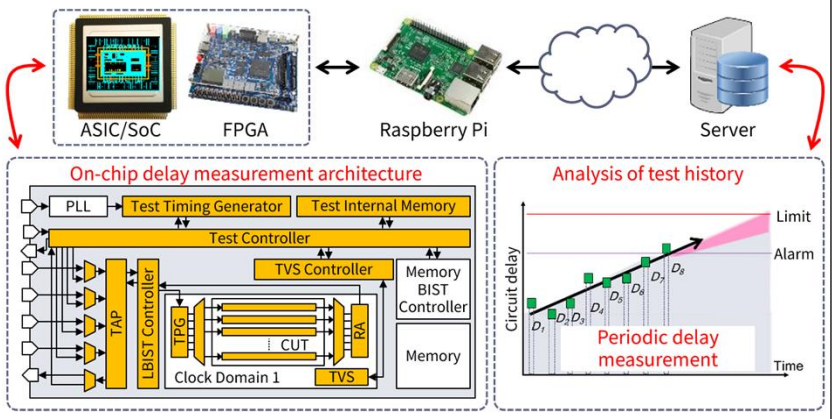

Fig. 1 On-chip delay measurement for field testing

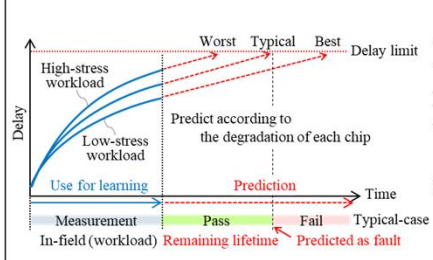

Fig. 2 Degradation prediction

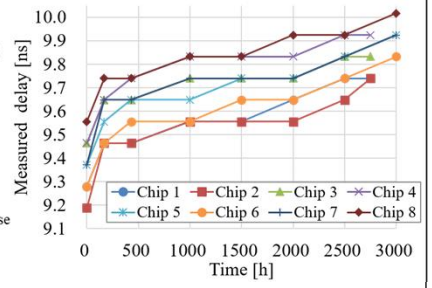

Fig. 3 Accelerated life testing for delay degradation

Content:

Failures caused by aging are increasing in state-of-the-art VLSI systems. Delay degradation can be detected by periodic in-field delay measurements after deployment, enabling prediction based on accumulated test history. However, circuit delays vary with temperature and voltage conditions, making on-chip digital temperature and voltage sensors essential for accurate, environment-independent measurement.

This work develops field testing technology for on-chip delay measurement (Fig.1) for delay degradation prediction based on reliability design and design-for-testability. We investigate delay measurement techniques considering process and operating variations, sensor self-calibration, and delay degradation prediction accommodating per-chip variations (Fig.2). The proposed methods are validated through simulations, prototype chips, and accelerated degradation tests (Fig.3), and are further applied to FPGAs using FPGA-oriented design and IoT-based evaluation.

Keywords: VLSI testing, delay test, design-for-testability, temperature sensor, FPGA

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