Faculty of Science and Technology
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Design for testability of VLSI chips

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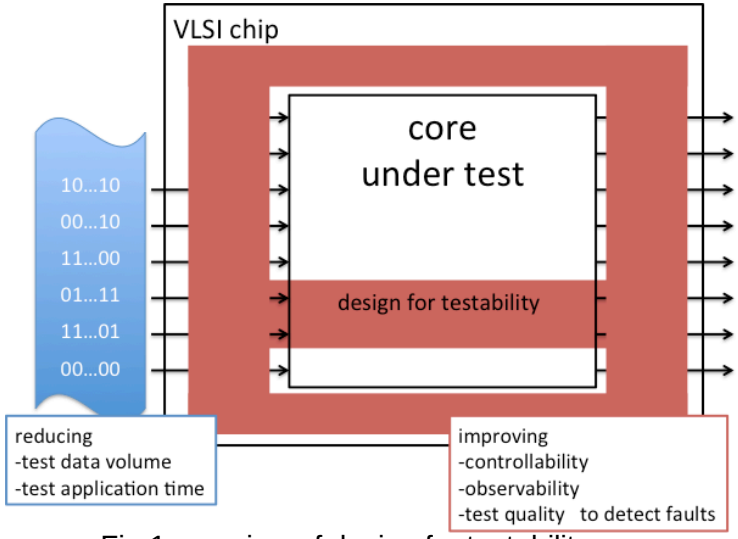

Fig.1 overview of design for testability

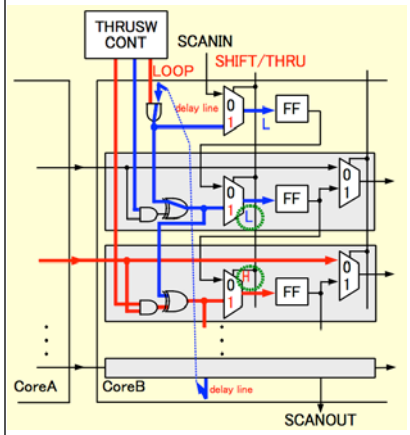

Fig.2 Boundary scan with TDC

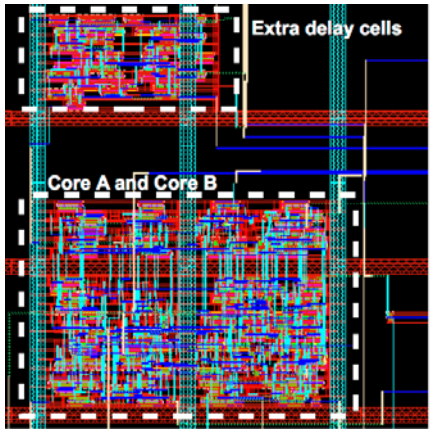

Fig.3 layout of an experimental chip

Content:

In recent highly integrated VLSIs, cost of testing is a major problem. To alleviate the difficulty in testing, design for testability techniques are widely used. In our research lab, we develop methods for reducing test cost such as test data volume, test application time, area overhead of test circuit, and for improving test quality especially in delay testing. One of the techniques is design for testability method for small delay faults using time-to-digital converter embedded in boundary scan called TDCBS, shown in the figures. The boundary scan cells are modified to be able to form a time-to-digital converter that is utilized for detecting delay. Using this architecture, defects like opens and shorts can be detected as extra delay caused by such defects even if the delay is small and cannot be detected by conventional logic test. The feasibility of the proposed methods is estimated by both simulation and experiments of fabricated chips.

Keywords: design for testability, VLSI testing, delay faults, test cost reduction

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