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Video coding algorithm and its VLSI architecture

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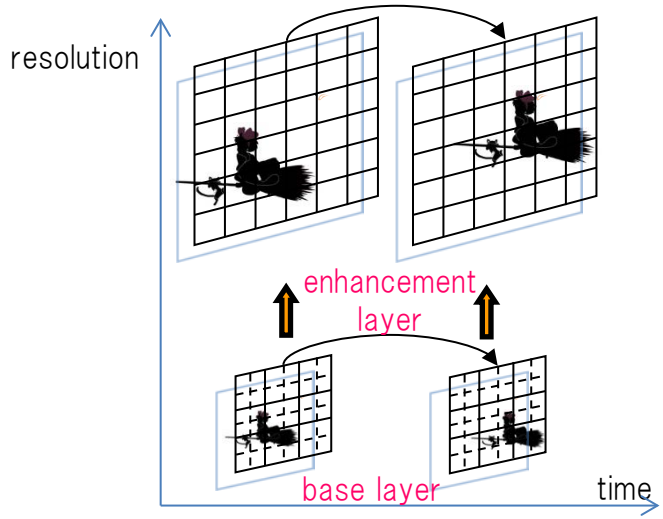

Fig.1: H.264/SVC inter layer prediction

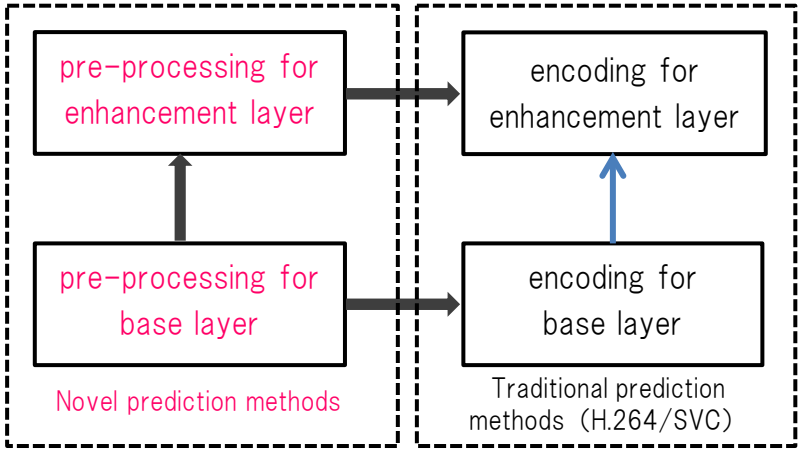

Fig.2: The proposed coding structure

With the widely spread of video applications, novel coding algorithms which can answer many kinds of emerging demands are highly required. Our research group is devoting to propose good ideas concerning the following themes.

1. Improvements of the algorithms of HEVC and its low complexity and low power VLSI architecture for the next generation applications which are over 4K resolutions. The algorithms and architectures are concerning the intra coding, motion estimation, and deblocking filter.
2. Scalable video coding algorithms which are suitable for high resolution applications. We will make full use of the high correlations between base layer and enhancement layer to propose new algorithms to improve the coding efficiency.
3. Highly parallel processing video coding algorithms on many core platforms. Most of traditional coding algorithms utilize the coding parameters of adjacent blocks to improve coding efficiency. However, this coding structure has essential demerit for parallel processing. As shown in Fig.2, our motivation is to find new coding structure which can achieve higher parallel coding performance.

Keywords : H.265/HEVC, Scalable Video coding(SVC), Parallel Video Coding

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