Faculty of Science and Technology
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# Video codec extension algorithm and its VLSI architecture using machine learning

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■ Prediction pixels generation using machine learning

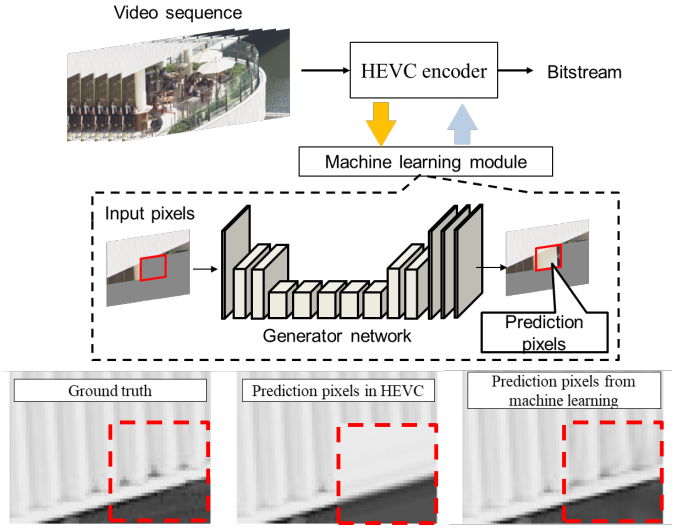


Fig. 1 Comparison of a conventional prediction pixels and proposed

■ LSI design of neural network for image processing

Represent complex neural network with ODE (Ordinary Differential Equation)

➡ Applicable to image processing

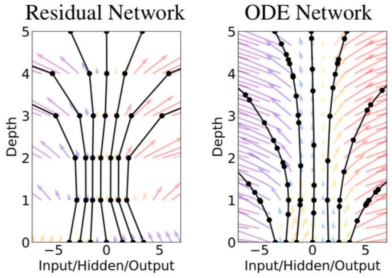


Fig.2 ResNet and ODE Net structure


Fig. 3 FPGA(PYNQ-Z1)

Content:

As the AI / IoT environment spreads to society, video will continue to play a major role as a technique of information transmission. In order to provide accurate and detailed moving images, video codec technology is implemented to various familiar devices. In the next generation codec technology, because parallel processing is difficult, an application to ultra-high resolution becomes more and more challenging. In this work, HEVC encoder is divided into two parts, an analysis circuit (machine learning module) and an encoding circuit (encoder) in order to establish a new encoding structure with high compression while achieving easy hardware implementation (Fig. 1). Predicted pixels value close to ground truth can be generated by embedding a machine learning module. In the future, we will implement FPGA of ODE Network to establish real-time processing of the image generation network (Fig. 2, 3).

By completing this work, we aim to make a significant contribution to the next-generation social infrastructure environment called AI, IoT, and 5G.

Keywords : Video coding, Machine learning, LSI design

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